

**BeagleBone A3 Port 8 Multiplexer table - A3 Printable - Revision 1**

PORT	PIN	PROC	NAME	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MODE7
P8_	1		GND								
P8_	2		GND								
P8_	3	R9	GPIO1_6	gpmc_ad6	mmc1_dat6						gpio1[6]
P8_	4	T9	GPIO1_7	gpmc_ad7	mmc1_dat7						gpio1[7]
P8_	5	R8	GPIO1_2	gpmc_ad2	mmc1_dat2						gpio1[2]
P8_	6	T8	GPIO1_3	gpmc_ad3	mmc1_dat6						gpio1[3]
P8_	7	R7	TIMER4	gpmc_advn_ale		timer4					gpio2[2]
P8_	8	T7	TIMER7	gpmc_oen_ren		timer7					gpio2[3]
P8_	9	T6	TIMER5	gpmc_be0n_cle		timer5					gpio2[5]
P8_	10	U6	TIMER6	gpmc_wen		timer6					gpio2[4]
P8_	11	R12	GPIO1_13	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in			gpio1[13]
P8_	12	T12	GPIO1_12	GPMC_AD12	LCD_DATA19	MMC1_DAT4	MMC2_DAT0	EQEP2A_IN			gpio1[12]
P8_	13	T10	EHRPWM2B	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpwm2B			gpio0[23]
P8_	14	T11	GPIO0_26	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpwm2_tripzone_in			gpio0[26]
P8_	15	U13	GPIO1_15	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe			gpio1[15]
P8_	16	V13	GPIO1_14	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index			gpio1[14]
P8_	17	U12	GPIO0_27	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpwm0_synco			gpio0[27]
P8_	18	V12	GPIO2_1	gpmc_clk_mux0	lcd_memory_clk	gpmc_wait1	mmc2_clk			mcasp0_fsr	gpio2[1]
P8_	19	U10	EHRPWM2A	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpwm2A			gpio0[22]
P8_	20	V9	GPIO1_31	gpmc_csn2	gpmc_be1n	mmc1_cmd					gpio1[31]
P8_	21	U9	GPIO1_30	gpmc_csn1	gpmc_clk	mmc1_clk					gpio1[30]
P8_	22	V8	GPIO1_5	gpmc_ad5		mmc1_dat5					gpio1[5]
P8_	23	U8	GPIO1_4	gpmc_ad4	mmc1_dat3						gpio1[4]
P8_	24	V7	GPIO1_1	gpmc_ad1	mmc1_dat1						gpio1[1]
P8_	25	U7	GPIO1_0	gpmc_ad0	mmc1_dat0						gpio1[0]
P8_	26	V6	GPIO1_29	gpmc_csn0							gpio1[29]
P8_	27	U5	GPIO2_22	lcd_vsync	gpmc_a8						gpio2[22]
P8_	28	V5	GPIO2_24	lcd_pclk	gpmc_a10						gpio2[24]
P8_	29	R5	GPIO2_23	lcd_hsync	gpmc_a9						gpio2[23]
P8_	30	R6	GPIO2_25	lcd_ac_bias_en	gpmc_a11						gpio2[25]
P8_	31	V4	UART5_CTSN	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd		uart5_ctsn	gpio0[10]
P8_	32	T5	UART5_RTSN	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3		uart5_rtsn	gpio0[11]
P8_	33	V3	UART4_RTSN	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3		uart4_rtsn	gpio0[9]
P8_	34	U4	UART3_RTSN	lcd_data11	gpmc_a15	ehrpwm1B	mcasp0_ahclr	mcasp0_axr2		uart3_rtsn	gpio2[17]
P8_	35	V2	UART4_CTSN	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2		uart4_ctsn	gpio0[8]
P8_	36	U3	UART3_CTSN	lcd_data10	gpmc_a14	ehrpwm1A	mcasp0_axr0			uart3_ctsn	gpio2[16]
P8_	37	U1	UART5_TXD	lcd_data8	gpmc_a12	ehrpwm1_tripzone_in	mcasp0_aclkx	uart5_txd		uart2_ctsn	gpio2[14]
P8_	38	U2	UART5_RXD	lcd_data9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd		uart2_rtsn	gpio2[15]
P8_	39	T3	GPIO2_12	lcd_data6	gpmc_a6		eQEP2_index				gpio2[12]
P8_	40	T4	GPIO2_13	lcd_data7	gpmc_a7		eQEP2_strobe	pr1_edio_data_out7			gpio2[13]
P8_	41	T1	GPIO2_10	lcd_data4	gpmc_a4		eQEP2A_in				gpio2[10]
P8_	42	T2	GPIO2_11	lcd_data5	gpmc_a5		eQEP2B_in				gpio2[11]
P8_	43	R3	GPIO2_8	lcd_data2	gpmc_a2		ehrpwm2_tripzone_in				gpio2[8]
P8_	44	R4	GPIO2_9	lcd_data3	gpmc_a3		ehrpwm0_synco				gpio2[9]
P8_	45	R1	GPIO2_6	lcd_data0	gpmc_a0		ehrpwm2A				gpio2[6]
P8_	46	R2	GPIO2_7	lcd_data1	gpmc_a1		ehrpwm2B				gpio2[7]

**Note:** The multiplexer states can be modified by writing over the file in `/sys/kernel/debug/omap_mux/#name#` where #name# is the mode0 of the pin  
 Command Line example to set Port 8 Pin 31 to uart5\_rxd  
`echo 4 > /sys/kernel/debug/omap_mux/lcd_data14`

**Source** Based on data in BeagleBone system reference manual RevA3\_1.0

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